Radiation Effects in Advanced Microelectronics Technologies[†]

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Abstract

The pace of device scaling has increased rapidly in recent years. Experimental CMOS devices have been produced with feature sizes below 0.1 μm, demonstrating that devices with feature sizes between 0.1 and 0.25 μm will likely be available in mainstream technologies after the year 2000. This paper discusses how the anticipated changes in device dimensions and design are likely to affect their radiation response in space environments. Traditional problems, such as total dose effects, SEU and latchup are discussed, along with new phenomena. The latter include hard errors from heavy ions (microdose and gate-rupture errors), and complex failure modes related to advanced circuit architecture. The main focus of the paper is on commercial devices, which are displacing hardened device technologies in many space applications. However, the impact of device scaling on hardened devices is also discussed.

I. Introduction

The evolution of integrated circuit technology has been widely discussed during the last decade, but relatively little attention has been given to the way that device scaling is expected to influence the performance of advanced devices in space. During the last five years, the "five-volt barrier" has been broken, and device scaling has proceeded along several different paths, allowing lower power supply voltages to be used as feature size diminishes.

For CMOS, two basic scaling approaches must be considered: (1) high-performance scaling (for devices like microprocessors) where much of the circuit operates at a high duty cycle, and speed, or combinations of speed and power are the main figures of merit; and (2) low-power circuits, where speed and overall performance are less significant than power requirements. Different scaling algorithms are necessary in order to optimize MOS devices for these two basic circuit design approaches.

It is also useful to add a third scaling category for memories. Memory technologies are somewhat concerned with access time, but the main consideration is minimizing standby power, because very little of the circuit is active at a given time, and large banks of these devices are usually required. Different scaling algorithms are used for memories than for more conventional CMOS circuits.

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The main emphasis of this paper will be on how device scaling affects the radiation response of unhardened commercial technologies, which are being used in many present and future space systems with less stringent radiation requirements. Commercial technologies are generally more advanced than hardened device technologies because of the increased resources and cost/performance pressure of the commercial marketplace. However, some aspects of device scaling also affect radiation effects in hardened technologies, and are also addressed in the paper to a more limited extent.

II. Scaling Scenarios

A. CMOS Scaling

Device scaling in the mid 1970's and early 1980's considered two basic approaches: constant voltage scaling, where the logic power supply voltage was assumed to be fixed at five volts; and constant-field scaling, where the voltage was allowed to scale with feature size [1,2]. These basic concepts worked surprisingly well as long as the power supply voltage was much larger than the gate threshold voltage and the limitations imposed by the subthreshold slope (which doesn't scale).

A great deal of subsequent work on scaling has been done in the device community [3-8]. This work has shown that device scaling is a highly complex problem requiring tradeoffs between many different parameters. New scaling algorithms are required for more advanced devices that consider hot carrier effects, subthreshold conduction, drain resistance, interconnects, contact technology and power dissipation. For example, Figure 1 after Davari, et al. [3], shows how stage delay (speed) is affected by power supply voltage for a 0.25 μm CMOS process. The stage delay increases rapidly as the voltage is reduced below 2 V, which is expected from elementary device performance considerations. Although increasing power supply voltage decreases the stage delay, this only occurs for voltages below 2.5 V because of the need for lightly doped drain (LDD) regions to reduce hot carrier effects at higher voltages. The LDD regions increase the series resistance. The net result is a minimum in the delay/voltage relationship. The three curves correspond to different voltage margins for hot-carrier reliability, and illustrate how various factors must be combined in order to arrive at final design tradeoffs in scaled devices.

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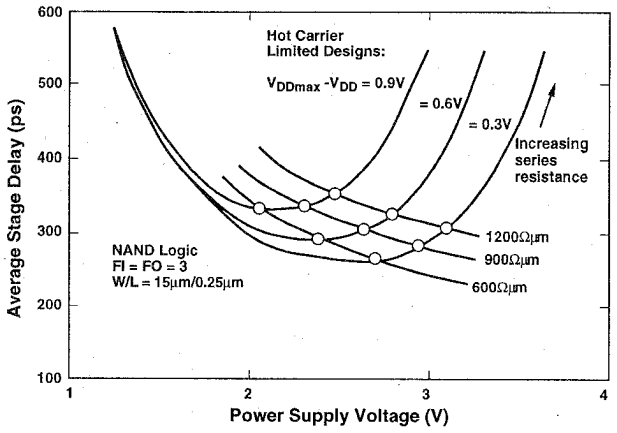

Figure 1. Speed/Reliability Tradeoff for a 0.25 μm CMOS Process *(after Davari, et al. [3])*

Many other parameters have to be considered in developing scaled devices. Table 1 shows predictions for device technologies with channel lengths between 0.9 μm and 0.07 μm [5], including high-performance and low-power scaling. Component density (essentially the relative number of devices that can be placed on a die with a specific area) is predicted to increase by approximately a factor of 50 by the year 2004 relative to devices in the late 1980's. Power supply voltages will be reduced for both scaling scenarios.

Table 1. CMOS Scaling Predictions

Parameter	Late 1980's	1992	1995	1998	2001	2004
Supply voltage (V)						
High performance	5	5/3.3	3.3/2.5	2.5/1.8	1.5	1.2
Low power	–	3.3/2.5	2.5/1.5	1.5/1.2	1.0	1.0
Lithog. resolution (μm)	1.25	0.8	0.5	0.35	0.25	0.18
Channel length (μm)	0.9	0.6/0.45	0.35/0.25	0.2/0.15	0.1	0.07
Gate oxide thickness (nm)	23	15/12	9/7	6/5	3.5	2.5
Relative density	1.0	2.5	6.3	12.8	25	48
Relative speed						
High performance	1.0	1.4/2.0	2.7/3.4	4.2/5.1	7.2	9.6
Low power	–	1.0/1.6	2.0/2.4	3.2/3.5	4.5	7.2

The values in Table 1 are deceptively simple. They are arrived at after trading off numerous factors that affect device design. Figure 2 provides additional insight into the process. It shows how the electric field in the channel region changes with scaling (the channel length is typically ≈ 60-80% of the minimum feature size). The electric field increases with scaling for both scaling scenarios compared to the older constant-field approach, but the increase is much stronger for the high-performance case. The scaling approach assumes that doping levels are modified to provide maximum drive current and low off current, and that the device structure also takes into account limitations caused by tunneling through thin oxides as well as tunneling in the high-field region of the drain. Highly scaled devices (feature size below 0.25 μm) do not use LDD structures in order to keep the device geometry small and to maintain low internal device resistance. The reader is referred to references [3-8] for more details.

B. Scaling and Space Radiation Effects

It is possible to identify specific areas relating to scaling that are expected to have the largest influence on the radiation performance of highly scaled devices. These are discussed in the following subsections.

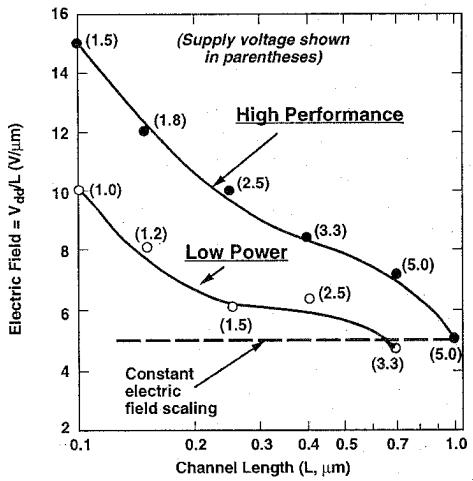

Figure 2. Predicted Evolution of Electric Field in the Channel Region with Scaling *(after Davari, et al.[3])*

Electric Field in the Gate Region

Although one might expect that lower electric field strength would occur in the gate regions of devices with lower power supply voltage, scaling predictions from the electron device community predict higher field strengths in order to optimize performance, provided that the breakdown characteristics of oxides can be improved [6,7]. This requires a reduction of the defect density within the oxide. Earlier scaling predictions were based on the assumption that 2 MV/cm was the maximum practical oxide field strength [2], but advances in fabrication technology have relaxed that limit. More recent work has shown that the breakdown characteristics of oxides below 100 Å are somewhat better than the breakdown characteristics of thicker oxides [6]. However, oxide quality is strongly affected by other processing steps [9], and oxide breakdown remains an important practical issue for scaled devices.

Figure 3 shows the predicted evolution of oxide field strength for high-performance and low-power scaling [3,6]. The horizontal scale provides constant intervals each time that the feature size is reduced by two, consistent with the concept of different generations of device technology. The results in Figure 3 are for optimized devices. Past history suggests that the initial generation of devices with a specific feature size will use field strengths that are somewhat lower than the optimized value. There are a number of reasons for this, including high risk to the manufacturer if the technology cannot be manufactured with sufficient reliability. Thus, actual device technologies may lag somewhat from predictions based on optimized values.

The practical limit to oxide thickness is 30-50 Å because of tunneling currents, which become significant for very thin oxides [6]. Alternative dielectric materials or sandwiched structures may be necessary in order to produce devices with thinner oxides.

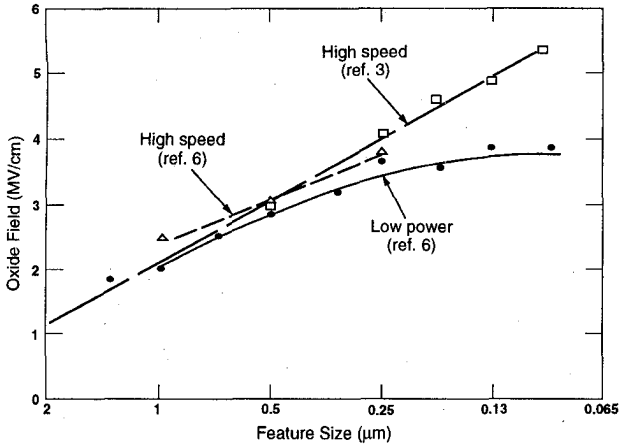

Figure 3. Projected Electric Field Across the Gate Oxide for Various Feature Sizes

Subthreshold Characteristics

One of the major difficulties in device scaling is that gate threshold voltage cannot be scaled with other parameters because of the subthreshold slope. Although this is a minor factor for power supply voltages in the 3-5 range, it has a major impact on device design when the power supply (and logic switching levels) are low. Subthreshold conduction characteristics cause the ratio of the "on" and "off" currents in an elementary logic element to be reduced for lower logic swings (i.e., lower supply voltage). This has several deleterious effects: (1) increase in leakage current, (2) reduced noise margin, (3) reduced circuit tolerance to statistical variations in device parameters, and (4) increased sensitivity to upset from alpha particles and high-energy particles.

For bulk CMOS, the subthreshold slope is approximately 80 mV/decade at 300 °K. A six decade on/off ratio then requires a threshold voltage of about 0.5 V.† This is an adequate ratio for high-performance devices, but a much larger ratio is usually required for memory circuits in order to maintain low overall operating current. The elementary argument above does not consider the effect of lower threshold voltage on more elaborate circuits. The subthreshold slope increases at higher temperature, further limiting the degree to which threshold voltage can be reduced and still maintain adequate operating margin.

One of the advantages of SOI technology is a reduction in subthreshold slope to approximately 60 mV/decade. This provides a major advantage for circuit design with low power supply voltages, and it is one reason that SOI is frequently discussed as a future competitor to bulk CMOS technology. Although higher fabrication and wafer costs have prevented SOI devices from being a factor in the commercial marketplace, SOI may become a mainstream technology in the longer term.

†The on/off ratio depends on circuit design, as well as on the actual subthreshold slope, which may be larger than 80 mV/decade. See references [3-8] for more details.

Doping Fluctuations

As feature sizes are reduced, the total number of dopant atoms used in the channel region to determine the threshold voltage decreases to the point that statistical variations in the number of atoms causes a significant spread in the subthreshold characteristics for the many transistors within a single integrated circuit [10,11]. Figure 4 shows the results of a simulation for a 1.5 V process with 0.07 μm feature size [11]; the gate oxide thickness was 30 Å. The coefficient of variation (σ/mean) of the distribution, is 0.06, leading to a 4-σ range in threshold voltage of nearly ±25%! For comparison, the 4-σ range of threshold voltage for a process with a gate oxide thickness of 150 Å is less than ±2% [10].

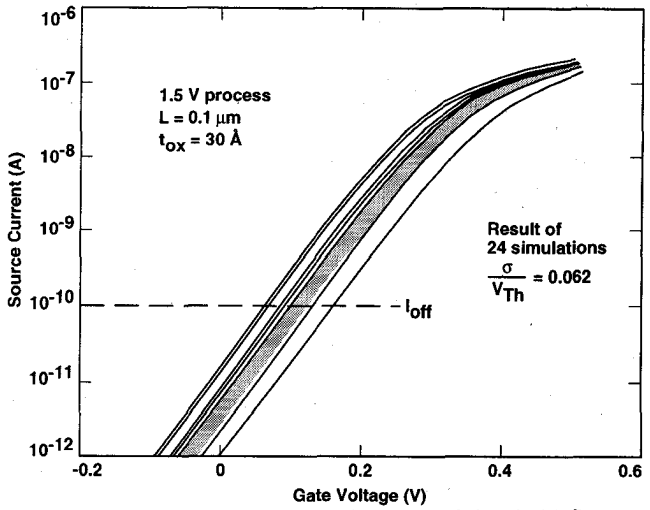

Figure 4. Effect of Doping Fluctuations on Subthreshold Current

The final effect on circuit design depends on the circuit operating margin as well as on the size of statistical fluctuations in threshold voltage. The extended slope of the subthreshold region reduces operating margins for circuits with lower power supply voltages, exacerbating the effect of doping fluctuations, and reducing the on/off ratio. This affects the optimization process, particularly for low-power designs which are more dependent on maintaining a uniform and acceptably high on/off ratio within the circuit. Thicker oxides may be required to reduce the impact of the doping fluctuation problem for low-power scaling; a thicker oxide requires a larger total number of dopant atoms for a given threshold voltage implant, reducing the statistical effect of doping fluctuations.

Doping Levels and Substrate Technologies

Nearly all advanced technologies are fabricated with a twin-tub CMOS process, which uses additional processing

steps to allow the doping levels of the well regions of the n- and p-regions in which MOS devices are actually placed to be tailored. This improves device performance compared to older processes, which used only a single well (usually an n-well). The bulk substrate in older technologies was used for the other (n-channel) MOS transistor type, accepting some performance limitations.

From the standpoint of device performance, substrate resistivity is not very important (except for latchup), and tends to be omitted in most discussions of scaling. However, the substrate resistivity and epitaxial layer thickness *under the twin-well structure* are very important for single-event upset, because of the influence of the substrate region on charge collection. Scaling theory predicts that the well resistivity will increase somewhat with scaling. There is potential confusion here because the doping level of the p-well in twin-tub processes is often referred to as substrate resistivity in the device literature.

Table 2 shows substrate doping levels for a variety of devices. The resistivity of the first four devices was obtained from spreading resistance measurements. Resistivity of the last two device types is taken from the literature. The key point is that although newer devices are made on epitaxial substrates, the resistivity has changed very little over a period of ten years. This is of critical importance in determining how scaling affects single-event upset.

Table 2. Substrate Doping Levels for Various Device Types

Circuit Type or Technology	Data Source	Sub. Type	Doping Level (atoms/cm^3)
4464 SRAM	Meas.	Bulk	8×10^{14}
HM65162 SRAM	Meas.	Bulk	2×10^{15}
32-Mb flash mem.	Meas.	Epi	8×10^{14}
K-5 processor, 5V	Meas.	Epi	$\approx 2 \times 10^{15}$
0.25 μm, 2.5 V	Literature	Epi	1×10^{16}
0.1 μm, 1.5 V	Literature	Epi	1×10^{16}

C. *Special Considerations for Memories*

Different scaling scenarios are required for memory technology than for logic circuits [12,13]. One of the main factors in memory design is leakage current from subthreshold conduction. The sheer increase in the total number of storage cells in very large memories makes it necessary to increase the allowable time period between refresh cycles, which depends on leakage current.

Another important issue is that of minimizing short-channel effects (SCE), which increase threshold voltage variations, affecting access time and sense amplifier offset. Increasing the substrate doping level (well doping level in twin-tub processes) helps to suppress SCE, but adversely affects leakage current because of tunneling.

Figure 5 shows how the cell area and stored charge of DRAMs are affected by scaling [14]. The cell area scales nearly exactly as the inverse of the memory capacity, reflecting miniaturization of individual transistors. However, the signal charge scales with a much shallower slope. This is due to several factors, one of which is the need to keep the stored charge well above the "noise floor" of alpha particles, which are present in metallization, capacitor materials, and other regions of the device. The charge produced by a 5 MeV alpha particle through a 1 μm path length is indicated in the figure for comparison.

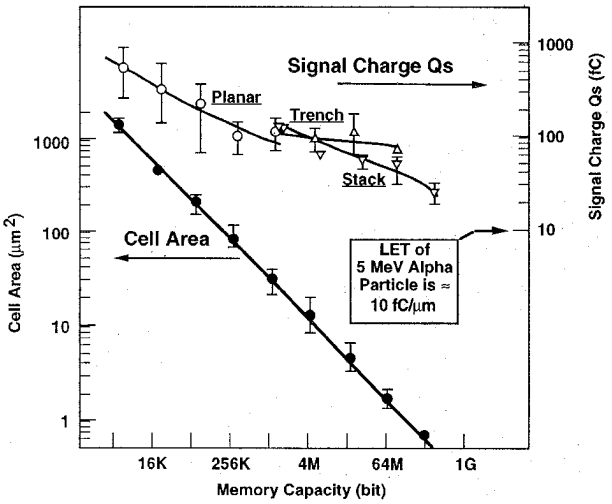

Figure 5. Transistor Size and Storage Capacitance Scaling for DRAMs *(after Lage, et al. [14]).*

Upset from alpha particles is a major concern for DRAMs as well as for SRAMs. Most manufacturers design and test their devices to make sure that the upset rate is below specific values, typically ≈ 100 FITs (one FIT = one failure in 10^9 operating hours). Thus, it is reasonable to assume that alpha upset conditions provide a lower bound to single-event upset sensitivity for most commercial devices. In the past, manufacturers performed accelerated testing with high-intensity alpha sources to verify adequate margin. However, the device community has recognized that the error rate can be much higher when the tests are done with a lower intensity source over longer time periods because of the contribution from cosmic ray interactions (principally neutrons) in terrestrial applications. Many manufacturers take this into account as well as the alpha upset problem [14,15], further increasing the "floor" for single-event upset.

III. TOTAL DOSE EFFECTS

A. *Gate Threshold Shift*

The threshold shift that results from hole traps in MOS gate oxides decreases as the square of oxide thickness, assuming that the hole trapping efficiency is unchanged as the oxide thickness is reduced [16]. Table 3 compares the

threshold shift expected for different device types at 10 krad(Si), assuming unhardened oxides with 50% hole trapping. It shows how scaling improves total dose hardness from the standpoint of gate threshold voltage changes caused by hole traps.

Saks has shown that tunneling affects hole trapping as the oxide thickness (t_{ox}) is reduced below 100 Å [17], reducing the trapped charge even further in highly scaled devices. That factor is not taken account in Table 3.

Table 3. Gate Threshold Voltage Shift from Hole Trapping at 10 krad(Si) for Various Oxide Thicknesses

Oxide Thickness (Å)	Representative Technology	ΔV_T @ @10 krad(Si) (mV)
1000	1970's CMOS; power MOSFETs	-1700
230	Late 1980's	-90
120	3.3-V process	-25
80	2.5-V process	-11
60	1.8-V process	-6

Although one would expect that hole trapping will not be very significant for devices with thin oxides, the situation is not that simple because of the increasing importance of gate voltage fluctuations discussed in the previous section. Gate oxide threshold shifts produced by hole traps will shift the subthreshold characteristics in the direction that increases conduction, increasing the "off" current.† This can be a significant issue for low-power devices (or for memories) with power supply voltages above 2 V, even though the voltage shifts are small. The nonscalability of the subthreshold slope reduces circuit margin, and relatively small shifts in threshold voltage can produce large changes in leakage current for devices near the statistical "edge" of the threshold voltage distribution within the circuit.

Hole traps in the gate region may still be important even for thin oxides in applications with very high total dose levels. In addition, a new total dose mechanism has been recently reported by Scarpa, et al. for ultrathin gate structures [18]. They observed that leakage currents in 44 Å gate oxides increased at total dose levels above 1 Mrad(Si). This is a new effect that may be important in selected applications. More work is required to determine the mechanisms that affect the leakage current and the influence of oxide processing on this effect.

†Ionizing radiation effects in CMOS are much more complicated than indicted above. Interface traps are produced as well as hole traps. The result is that threshold voltage shifts can be either positive or negative in n-channel devices (see reference 16 for a more complete discussion). However, the point of the above discussion is that trapping in gate oxides becomes insignificant for most devices as gate oxides are reduced in accordance with scaling predictions.

B. High-Voltage Requirements and Special Circuit Functions

Even though the general impact of scaling is to reduce the effect of gate threshold shifts as devices are scaled to the point where tunneling reduces hole trapping, some device technologies --such as flash memories -- require selective use of higher internal voltages, which in turn require thicker gate oxides, at least for the devices that must switch and control the higher voltage. The requirement for such circuitry is not always apparent from device specifications. Many complex circuits use internal charge pumps either to provide high internal voltages, or to provide a slightly boosted internal voltage condition for startup or switching purposes.

Charge pump circuits typically operate at low currents, and are often much more affected by small threshold shifts than logic circuits. Degradation of the charge pump can have a major impact on overall circuit operation. For example, Katz, et al., found that total dose degradation of the internal charge pump in a programmable gate array caused the external power supply current to increase from a few mA to nearly 1 ampere [19]! This occurred at a total dose level of 12 to 18 krad(Si), and persisted until self-heating annealed the part to the point where normal operation was possible. Upon continued irradiation, the part reverted to the high-current state. In this case the charge pump was used to provide an additional bias voltage to internal logic elements in the array. The excess current was caused by partial turn-off of internal transistors that are normally used only for programming, and cause partial turn-on of internal logic. The programming transistors are normally off, with an internal voltage derived from the charge pump.

Another example is shown in Figure 6, for a modern flash memory. This particular flash technology requires an internal voltage of 12 volts to erase and write to the memory cells, derived from an internal charge pump. The external power supply voltage is five volts. Total dose degradation increased the time required to write to the device from less than one second to more than 600 seconds at 20 krad(Si). The "write" mechanism in this part is hot-carrier injection from the drain region, which is highly sensitive to voltage. Degradation of the internal charge pump circuitry caused the large increase in write time. None of the other parameters of the memory were affected.

These examples not only show the importance of charge pump degradation, but also illustrate how such degradation can affect circuit functions in unexpected ways. It is possible to inadvertently miss these effects unless total dose tests are done carefully and thoroughly. For example, in the FPGAs discussed above, the huge current could be missed if in situ monitoring was not used, and if the part annealed during the

time between successive irradiation steps. The excess current first shows up as a startup problem well before operational current increases are observed.

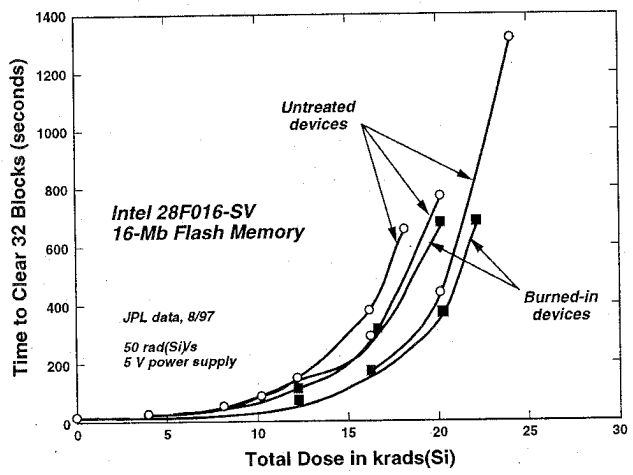

Figure 6. Effect of Total Dose on Write Time for a Flash Memory

C. *Field Oxides*

Although scaling is expected to reduce gate threshold voltage effects to the point where it is no longer important, charge trapping in the thick field oxides that are used in CMOS processes is still a significant issue. For many devices field oxide inversion is the dominant response mode, even for devices with feature sizes in the 0.8 to 2 μm range. The radiation level at which such changes occur has increased somewhat for more advanced devices, consistent with trends in field oxide thickness. The field thickness of older devices was > 1000 nm. This has been reduced to 300-600 nm in newer technologies. However, the geometry of the "bird's beak" region of field oxides makes it more difficult to determine how charge trapping affects the isolation characteristics compared to gate oxides. It is not simply related to the oxide thickness, but depends on the geometry.

A two-dimensional model for charge trapping in field oxides has been developed by Escoffier, et al. [20]. Figure 7 shows an example of their results, along with the structure that they simulated. A two-dimensional simulator was required for the calculations. Note that the maximum trapped charge density occurs in the transition region, where the oxide has intermediate thickness. Their work shows that the slope of the transition region and the doping level underneath the oxide both affect charge trapping in field oxides. More recent work by Brisset, et al. has extended field oxide modeling, studying the effect of different isolation oxide contours on charge trapping [21]. They showed that significantly more hole traps occur for oxides with steeper contours. This suggests that field oxide inversion may be a more difficult problem for scaled devices with sharper transitions between the gate and isolation oxides. Flament, et al. obtained similar results for the location of hole traps in LOCOS structures [22].

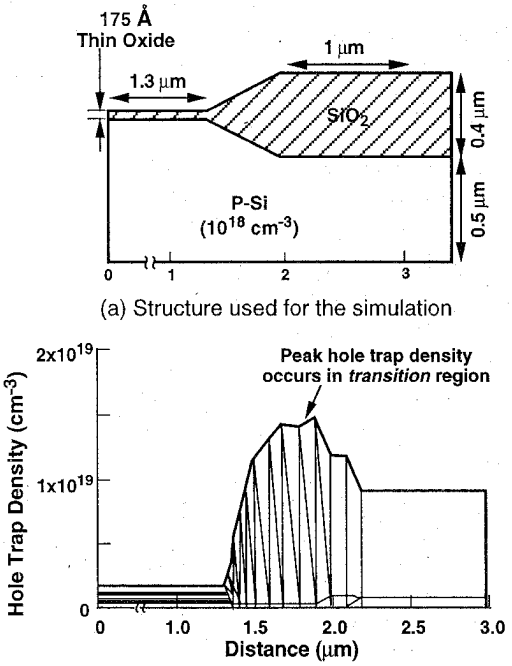

Figure 7. Simulated Charge Distribution in Field Oxides [20].

It is difficult to get specific information about field oxides for advanced processes. Field structures are rarely included in discussions of scaling and device performance. In some cases equivalent devices from different manufacturers have widely different sensitivity to field-oxide degradation. This area needs to be investigated more thoroughly for COTS devices.

Doping levels are expected to increase somewhat as devices are scaled to smaller dimensions, with some improvement in the radiation hardness of field oxides. Test results on DRAMs over the last five years show that the radiation level for abrupt increase in power supply current (assumed to be due to field oxide inversion) has approximately doubled for 64-Mb devices compared to 4-Mb technology. However, the radiation level for field-oxide inversion of microprocessors from one manufacturer have changed very little during the last ten years as the device technology evolved, indicating that one cannot necessarily count on improved field-oxide performance from scaling.

Lateral encroachment of the "bird's beak" structure forces modifications to the isolation process for feature sizes below 0.6 μm. Various approaches have been proposed to reduce the lateral geometry of LOCOS isolation, including poly buffered LOCOS [23], and polysicilon-encapsulated local oxidation [24]. Conventional LOCOS and an advanced poly-buffered are compared in Figure 8, below. The advanced process uses a recessed oxide and lateral nitride layer along with a sacrificial polysilicon layer. The radiation response of advanced isolation methods has not been examined, but the smaller dimensions and higher fields may make the radiation-induced inversion problem worse.

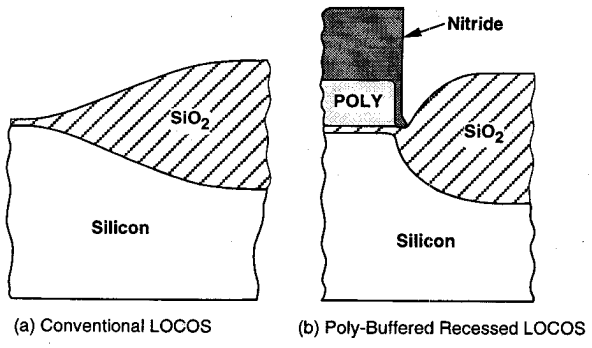

Figure 8. Diagram of Conventional LOCOS and an Advanced LOCOS Process

More advanced devices with feature sizes below 0.25 μm will use shallow trench isolation instead of conventional oxides [25]. Although no radiation modeling has been done to date on shallow trench regions, the work of Brisset, et al. on oxide contours suggests that the abrupt transition region in trench technology may be more susceptible to inversion than older (LOCOS) isolation methods. Additional work is needed to improve the understanding of ionization effects on advanced isolation technologies.

IV. Single-Event Upset

A. *Basic Models and Elementary Scaling*

Most early work on single-event upset was done with basic static memories. Many of the concepts used in SEE modeling (such as the concept of a constant charge collection volume with simple geometry) used today are based on this work. As discussed later, charge collection and geometrical effects in more modern devices are more complex, and it is probably unrealistic to expect these simple concepts to hold for advanced devices. This makes the scaling issue more difficult to address for SEE phenomena.

With the assumptions that are inherent in the basic RPP model [26,27], critical charge is expected to decrease as feature size diminishes. The solid line in Figure 9 shows an earlier projection, which held for different device technologies in the early 1980's [28]. Most of these devices were fabricated on bulk substrates, with feature sizes above 2 μm.

More recent results suggest that the concept of SEE scaling is quite different for more advanced commercial devices. For example, Table 4 shows the threshold LET for commercial microprocessors over an eleven-year time period [29-34]. These devices evolved rapidly, with feature sizes that ranged from about 1.5 to 0.35 μm (the feature sizes in this table are approximate). Clearly there is little difference in the threshold LET, even though device scaling was a key factor in increasing the speed and functional capability of these devices.

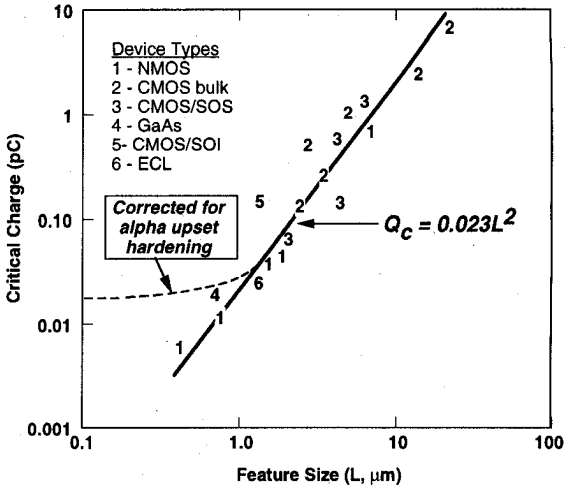

Figure 9. Relationship Between Feature Size and Critical Charge (*after Petersen, et al. [28]*)

Table 4. Upset Threshold of Microprocessors over an Eleven-Year Time Period

Device	Manuf.	Year	Feature Size*(approx.)*	Threshold LET (MeV-cm²/mg)
Z-80	Zilog	1986	3 μm	1.5-2.5
8086	Intel	1986	1.5 μm	1.5-2.5
80386	Intel	1991	0.8 μm	2-3
68020	Mot.	1992	0.8 μm	1.5-2.5
LS64811	LSI	1993	1.2 μm	2-2.5
90C601	MHS	1993	≈ 1.2 μm	2-2.5
80386	Intel	1996	0.6 μm	2-3
PC603E	Mot.	1997	0.4 μm	1.7-3
Pentium	Intel	1997	0.35 μm	2-3

The likely reason is that these devices are already near the practical limits of SEE sensitivity from the standpoint of sensitivity to upset from alpha particles and/or atmospheric neutrons. Most manufacturers consider these effects in designing their products, and verify that the upset rate is below a specific value (such as 10 FITs) with alpha-particle test data [14,15]. An LET upset threshold of 2-3 with heavy ions is consistent with such an approach, assuming margins of about 2 relative to alpha sensitivity to account for temperature effects, non-normal incidence, and some design conservatism. This suggests that the threshold LET of many commercial parts is near limits inherent in the manufacturing process, and hence is not likely to be lowered further by device scaling. Thus, the dotted line in Figure 9 is probably more representative of SEE trends for scaled commercial devices, compared to the original interpretation.

Although this elementary discussion considers threshold LET, it does not take into account how the cross section increases with LET or how the device responds and recovers

to SEE effects. Multiple-bit upset is also an issue for many devices [35,36]. For commercial devices the predictability and ease of correction at the system level are often the most important aspects of the SEU response. This depends on many factors, including device architecture (see Section VIII).

Another way to examine scaling effects is to compare the charge required to switch a basic CMOS inverter with minimum feature size as devices evolve. Figure 10 shows the results of such a calculation for two scaling scenarios, assuming that the load capacitance is twice the gate capacitance (light loading, with some allowance for interconnections). This figure shows that devices with feature size above 0.25 μm require switching charge that is well above the "alpha limit." However, that will no longer hold as devices approach feature sizes of 0.1 μm.

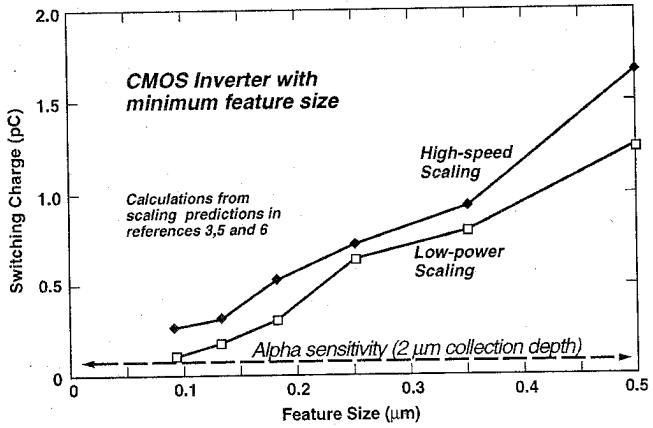

Figure 10. Effect of Scaling on Switching Charge of a CMOS Inverter with Minimum Feature Size.

Another important issue for more advanced devices is the way that the cross section varies with LET. Weibull distribution functions are often used to describe the dependence of cross section on LET [26,27]. Although this is a convenient way to incorporate the LET dependence, it is not based on any underlying physics, and can lead to major discrepancies if the data set used for characterization is limited. Figure 11 shows an example of a cross section for a 4-M DRAM where the cross section at low LET departs from the smooth curve that would be expected from the usual extrapolation methods. This makes a significant difference in the calculated error rate in applications such as solid-state recorders where large numbers of devices are required, and upsets from low LET particles make large contribution to the upset rate.

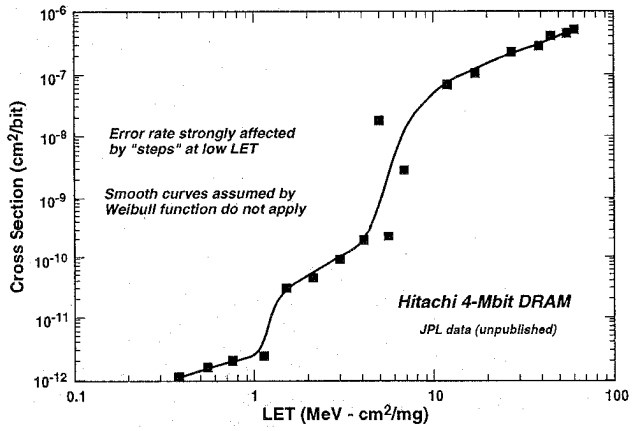

Figure 11. Cross Section for a 4-Mb DRAM Showing Structure at Low LET

B. *More Advanced Modeling*

Several groups have used computer modeling to study charge collection in more detail. This work has involved detailed cell structures as well as charge collection in elementary diodes. Dodd, et al. have demonstrated that the older concepts of a fast drift/funneling region followed by a slower diffused region do not really apply; instead, there is a continuous transition between "fast" and "slow" processes that depends on doping level [37]. They also showed that a significant contribution to the total charge occurs from charge generated in the substrate for epitaxial structures. This requires that we reexamine the assumption about how charge collection is related to epitaxial layer thickness.

A three-dimensional study by Woodruff and Rudeck showed several interesting effects that force one to reconsider the concept of critical charge, as well as how irradiation with ions at other than normal incidence affect SEE sensitivity [38]. The structure that they studied used a 5 μm eptiaxial layer on a highly doped substrate. The feature size of the process was 1.2 μm. The channel length of the transistor was 1.2 μm, with a total drain length (along the axis) of 3.5 μm. Figure 12 shows how the CMOS inverter that they studied responded to an ion strike with the same LET, but at positive and negative angles. The ion strike was placed at the center of the drain; a positive angle denotes a strike where the lower region of the track is closer to the source. There is a very significant difference in the response for positive and negative angles. With an LET of 50 MeV-cm²/mg, the cell would not upset at normal incidence or at negative angles up to 60°. When the simulation was done with *positive* angles, no upset occurred at 30°, but upsets occurred at 45° and 60°.

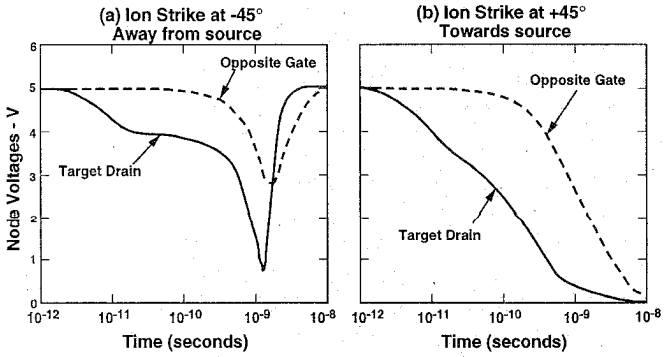

Figure 12. Drain and Gate Waveforms of CMOS Inverter Irradiated at Positive and Negative Angles [38].

They attributed these differences to charge generated from the source. Their simulations showed that the potential gradient of the funnel allowed electrons from the source to be injected into the charge column. Because of this effect, the total charge collected in the drain and substrate was actually greater than the charge deposited by the ion. Table 5 shows the total collected charge for various angles. Note that cell upset only occurred for angles above 30°, in the direction towards the source. Even though upset occurred at +45°, the simulation shows that no upset occurred with a -60° angle because the total collected charge is actually less. Additional work on charge collection in scaled device structures has been done by Velacheri, et al., who referred to the excess charge as ion-triggered channeling (ITC) [39], as well as by Dodd, et al. [40].

Table 5. Comparison of Deposited and Collected Charge for Ions with Different Incident Angles

Phenomenon	Angle of Ion Strike					
	+60°	+45°	+30°	0°	-45°	-60°
Deposited Charge (pC)	5.0	3.5	2.9	2.5	3.5	5.0
Collected Charge (pC)	14.8	10.1	7.6	5.7	6.0	7.9
Cell Upset	Yes	Yes	No	No	No	No

Three-dimensional simulations show that the conventional view of a simple charge collection region with fixed geometry for single-event upset is likely to fail when applied to more advanced device structures. They illustrate some of the difficulties that must be overcome in order to develop SEU-hardened technologies [38-41]. Even though this is a complicated problem, a number of hardened processes and designs are available with very low upset rates [42-44]. Hardened technologies are usually required for critical functions, such as flight computers and critical memory storage.

V. LATCHUP

Commercial devices are carefully designed to reduce sensitivity to electrically induced latchup from transients at input/output pins and power supply sequencing. However, they generally do not consider latchup from transients generated *within* the device, such as those produced by heavy ions or protons. Epitaxial substrates are widely used in scaled devices to help reduce latchup sensitivity in commercial technologies.

Layout and design rules play a major role in latchup susceptibility. These factors are not specifically included in the more generalized scaling discussions in the device literature, which makes it more difficult to address the issue of how scaling affects radiation-induced latchup. Special fabrication techniques -- such as trench isolation, retrograde wells, and SOI -- can be used to further reduce latchup susceptibility, but they have not been widely used in the past for high-volume commercial circuits because of cost. However, as discussed earlier, shallow trench isolation will likely be the mainstream isolation method for devices with feature sizes between 0.1 and 0.25 μm.

There is a wide variation in the latchup sensitivity of commercial devices to heavy ions. Figure 13, adapted from a thorough study by Chapuis, et al. [45], shows how the latchup threshold LET varies with epitaxial thickness for several different commercial device types. First-order theory, assuming consistent design, predicts that the minimum triggering conditions should depend on the reciprocal of the epitaxial thickness. The dashed line in the figure shows that this is roughly obeyed by a subset of the devices, but there are notable exceptions. This is hardly surprising, given that the devices were obtained from many different manufacturers. It illustrates that although epitaxial layers generally provide improvement compared to bulk devices, the use of epitaxial substrates cannot be counted upon to eliminate latchup or even to raise the threshold LET to values above 30 MeV-cm^2/mg.

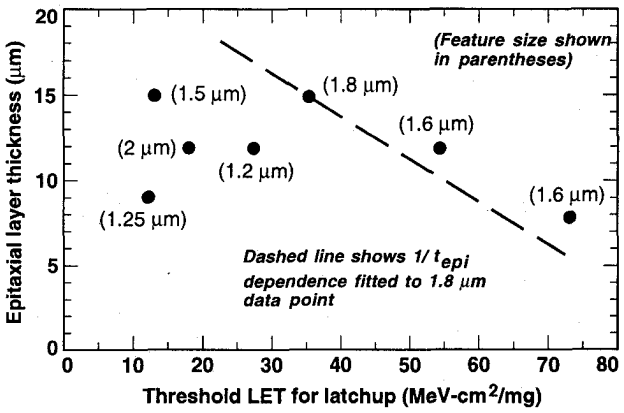

Figure 13. Relationship between Threshold LET and Epitaxial Thickness for Several Commercial Devices *(adapted from data of Chapuis, et al. [45])*

Many advanced devices are produced with very shallow epitaxial substrates, approximately 2.5-3 μm thick, much shallower than the devices represented in Figure 12. Work in our laboratory during the past two years has shown that most commercial devices built on such substrates will not latchup from heavy ions, even at LET values ≈ 100 MeV-cm^2/mg, indicating that device scaling will generally improve latchup resistance. However, a dramatic counter-example is provided by the K-5 processor [46]. As shown in Figure 14, this device has an extremely low latchup threshold, approximately 0.4 MeV-cm^2/mg; in fact, it is among the most sensitive of all commercial devices to radiation-induced latchup. It is fabricated on a very shallow epitaxial layer, approximately 2.5 μm thick, comparable to that of many other commercial devices which have not latched from heavy ions.

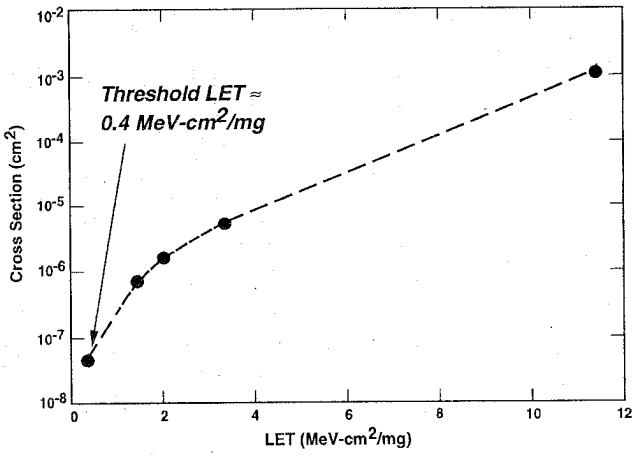

Figure 14. Latchup Cross Section for the AMD K-5 Processor

The K-5 result shows that epitaxial substrate construction cannot be used as a reliable indicator of latchup vulnerability. Clearly using shallow epi-layers helps to reduce latchup sensitivity, but other facets of the problem are also important. Latchup will likely remain an important issue for scaled devices until power supply voltages are reduced below 1.5 V, which is below the holding voltage of most latchup structures. However, latchup may still occur in low-voltage circuits that use internal charge pumps, and it is difficult to make generalized predictions of the effects of scaling on the latchup problem. Latchup is discussed in more detail in references [46-49].

VI. Microdose Hard Errors

Microdose hard errors were first observed by Kóga, et al, in 1991 [50]. Dufour, et al. did a more thorough study of hard errors during heavy-ion tests of 1-Mb SRAMs [51]. They reported that a small number of permanent errors occurred after irradiation with ions of very high LET (64 MeV-cm^2/mg in SiO_2). The errors recovered when the devices were annealed at high temperature, or when they were exposed to ultraviolet light. They attributed this to localized *microdose* from one or two heavy ions that struck the gate.

A later paper showed that the effect was consistent with the geometry of the SRAM and the hole trapping efficiency expected from heavy ions [52]. That work also predicted that microdose errors would eventually become less significant because of changes in SRAM memory technology, although it would continue to be an important issue for DRAMs. They assumed power supply voltages in the 3.3 to 5 V range in their analysis.

As discussed in Section II, much lower power supply voltages are being considered for near-term scaling, which will increase the importance of microdose errors because of subthreshold leakage. Another factor is circuit design; many low power design approaches depend on maintaining a high on/off ratio, and are more sensitive to voltage shifts than high-performance circuits.

One way to determine its importance is to compare the voltage change expected from a single microdose interaction with the range of statistical fluctuations that result because of doping fluctuations. Figure 15 shows how these effects compare, using scaling values from Table 1. There is a transition at approximately 2 V where the two contributions are equal. For devices below that voltage that are designed to the scaling rules predicted by the device community, microdose errors are not expected to be a significant problem, even for low-power devices. Above 2 V, microdose voltage shifts may cause significant problems for some circuits.

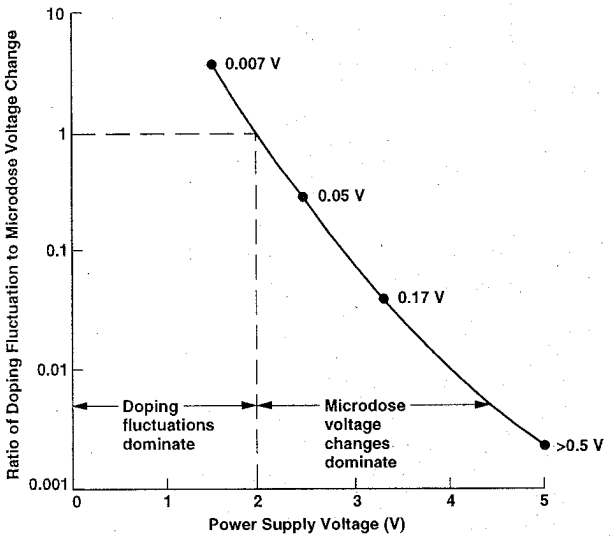

Figure 15. Comparison of Microdose and Dopant Fluctuation Contributions for Scaled Devices

Care must be used in interpreting Figure 15. It only holds for devices that use low voltages near their optimum scaling design point, not for arbitrary applications of devices with other optimization parameters to low-voltage designs.

VII. Gate Rupture Hard Errors

A. *Catastrophic Hard Errors*

Although microdose errors will probably become insignificant for highly scaled devices, that may not be the case for a second type of hard error, attributed to gate rupture. Gate-rupture errors were first reported by Swift, et al., during tests of 4-Mb DRAMs in 1994 [53]. They used DRAM retention-time characteristics to distinguish between microdose errors, which caused a statistical shift in the distribution of the retention time characteristics; and true hard errors (assumed to be caused by gate rupture) that caused the retention time to drop to very low values. These results are shown in Figure 16. The second type of error not only produced short retention times, but also produced errors in both the "1" and "0" conditions for the specific locations that were affected. Microdose errors only caused "0" errors, consistent with increased leakage from subthreshold conduction in the pass transistor.

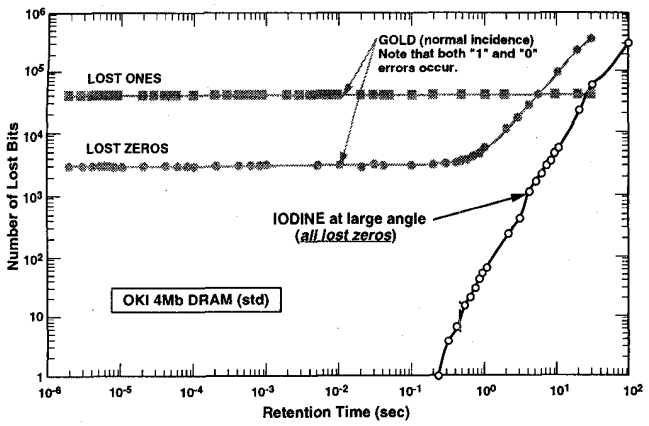

Figure 16. Retention Time Characteristics of DRAM Showing Evidence for Gate-Rupture Hard Errors [53]

The threshold LET required to produce hard errors in DRAMs is sufficiently high to keep the effect from being significant for 4-Mb DRAMs in typical space applications, but data on scaled devices showed that the threshold LET decreased, suggesting that the effect would likely become more significant for more advanced devices. Only some types of 4-Mb DRAMs were susceptible to gate-rupture errors, indicating that differences in the manufacturing process played a role in the process. Since that time, gate rupture errors have also been observed for a 16-Mb DRAM. Evaluation of 64-Mb devices has been slowed down because of difficulty in removing the top region of the package, which is usually required for heavy-ion tests.

Similar hard-error effects were also observed in field-programmable gate arrays [54]. Just as for the DRAMs, errors in the FPGAs occurred with normal biasing but the region in which the damage occurs is an oxide-nitride-oxide (ONO) sandwich, not a gate oxide. Unlike the DRAMs, the ONO insulator has no underlying silicon region. The manifestation of the effect was more difficult to detect in the gate arrays. For the FPGAs, hard errors "burned" the antifuses, causing additional gates to be selected. Although in principle this could be determined by an exhaustive check of the FPGA, in practice only a fraction of the gates within the array are used, and it would be very awkward to detect individual hard errors dynamically, during irradiation, with this approach. However, most of time an internal logic conflict arises when an extra gate is inadvertently programmed, and these conflicts produce small increases in the power supply current that appear as a series of steps during irradiation. That method was used to detect hard errors in the FPGAs.

DRAMs and FPGAs both contain large numbers of components, and one can get extra information about the nature of the mechanism by examining the way that errors on a specific device build up during irradiation. Figure 17 shows how the FPGA errors depend on the power supply voltage that is applied during the irradiation. The voltage dependence is quite strong. The cross section increases by more than three orders of magnitude for devices irradiated with power supply voltages of 4.5 to 5.4 V. Even more important, the dependence flattens out at a cross section that is more than one order of magnitude below the total area of the antifuses in the array. This suggests first that only "weak" structures are important at low voltages; and second, that several ion hits - 5 to 10 - are required in order to damage the more robust cells, near saturation.

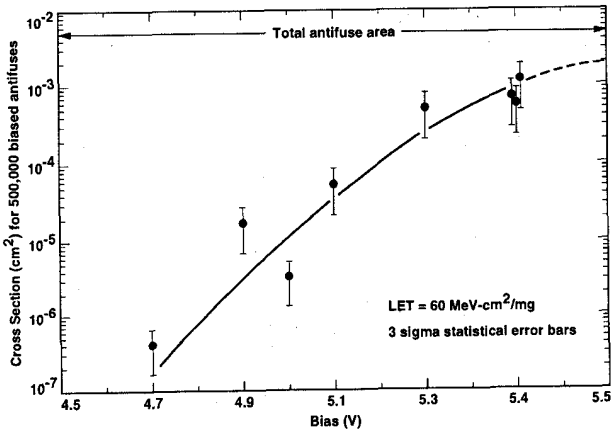

Figure 17. Dependence of the Number of Hard Errors on LET for an FPGA with ONO Anitfuses

The electric field at which the hard errors were observed in the 4-Mb DRAMs was 2.4 MV/cm for a device with 0.8 μm feature size, and 2.8 MV/cm for the device with 0.6 μm feature size (uncorrected for built-in potential). For the FPGA technology, the equivalent field strength (taking the dielectric constants of the ONO sandwich into account) was about 5 MV/cm (without considering built-in potential).

The potential impact of these types of hard errors on future device technology was discussed in a paper at the RADECS95 Conference [55], using DRAM results as a predictor. This work suggested that hard errors could become a major problem if the threshold LET for gate rupture continued to decrease with scaling. The work also pointed out that more work was required to determine the mechanisms, as well as the impact of other factors on gate rupture.

B. Gate Rupture in Capacitors

Sexton, et al., examined gate rupture in capacitors with different oxide thicknesses [56]. These were fabricated with several different CMOS processes, with oxide thickness ranging from 60 to 180 Å. They found that much higher electric fields were required to initiate gate rupture in the capacitors (6-9 MV/cm) than that reported in the earlier work on DRAMs, and also that the electric field increased for capacitors with thinner oxides.

Although the main focus of their work was on capacitors, they also examined gate rupture in SRAMs. However, the

SRAMs were not always fabricated with the same processes used for the capacitors. They found that the electric field required to initiate SEGR in the integrated circuits was about 30% lower than that required for the capacitors. Two different SRAMs were used, 16-kB and 256-kB; the field required by the larger SRAM appeared to deviate the most from the capacitor results, although they did not have capacitors from that particular process. They did not report cross sections for gate rupture in any of their experiments, only the LET at which breakdown occurred (≈ mA currents). Although their work indicates that gate rupture may become less significant for devices with very thin oxides, data from other laboratories has shown that gate rupture can occur at far lower electric fields than the devices in their study.

We have examined capacitors from a different process, using two different oxide thicknesses, 45 and 75 Å. As shown in Figure 18, the critical field for breakdown in our capacitors (corrected for contact potential) is considerably lower than for the capacitors tested by Sexton, et al. For example, the critical field for the 75 Å devices in our study was about 2/3 that of the 65 Å devices that they tested. At high LET, breakdown in the 75 Å devices occurred with an *applied* voltage of 4.6 V; breakdown in the 45 Å devices occurred with an applied voltage of 3.3 V. The difference in results for the two groups may be due to processing differences. Although that is not unexpected, it makes it difficult to establish definite trends for the effect of scaling on the gate-rupture problem, or to determine its net importance at specific oxide thicknesses and field strengths.

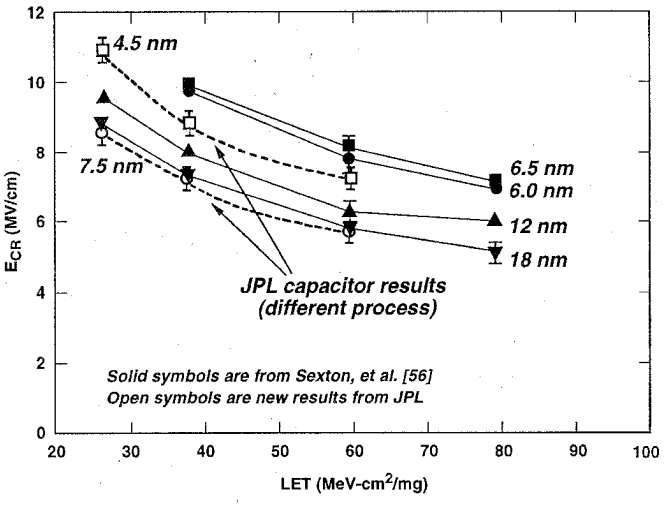

Figure 18. Dependence of Critical Field for Gate Rupture on Electric Field for Capacitors Fabricated with Integrated Circuit Technologies.

The area of the capacitors in our study was 0.003 to 0.011 cm^2. We noted that a large number of ions -- approximately 500 to 2000 -- had to pass through the capacitor before breakdown occurred. The breakdown appeared to be "soft," and was on the order of 20-100 nA for all devices, much lower than the currents used in the Sandia work. Multiple breakdowns could be observed on capacitors during most runs. The "soft" nature of the breakdown creates some ambiguity in evaluation of rupture-like effects in devices and in the comparison of data between different laboratories. It may be one reason for the difference between critical fields in the capacitors and memory devices that were studied by the Sandia group.

C. *Oxide Breakdown*

Oxide breakdown has been widely investigated by the device community, mainly from the standpoint of time-dependent dielectric breakdown. Most studies have used DC or low-frequency stress conditions. Many years of research have shown that this type of breakdown depends on the total charge that is injected into the oxide. Such studies usually inject charge in a relatively uniform manner over a large area, unlike charge from a heavy-ion track. Soft breakdown characteristics that are similar to the effects observed in irradiated capacitors by JPL have been reported in reliability studies of thin oxides under constant voltage stress [57].

A recent paper by Hu discussed oxide scaling from the standpoint of conventional reliability [58]. His work shows that it is possible to use thinner oxides in scaled devices than assumed by the scaling projections provided in Table 1. He projects the use of field strengths between 5 and 6 MV/cm for oxides between 30 and 80 Å. This is very close to the field strength where gate rupture occurred in the capacitors tested by JPL, but comfortably below the field strength required to initiate rupture in the capacitors tested by Sandia. This suggests that gate rupture may continue to be an important problem even for very thin oxides for some processes.

Biasing conditions may also play a role in the way that gate rupture is affected by scaling. For example, Figure 19 shows how the charge-to-breakdown (Q_{BD}) varied with biasing [59]. For oxide thicknesses above 80 Å, positive and

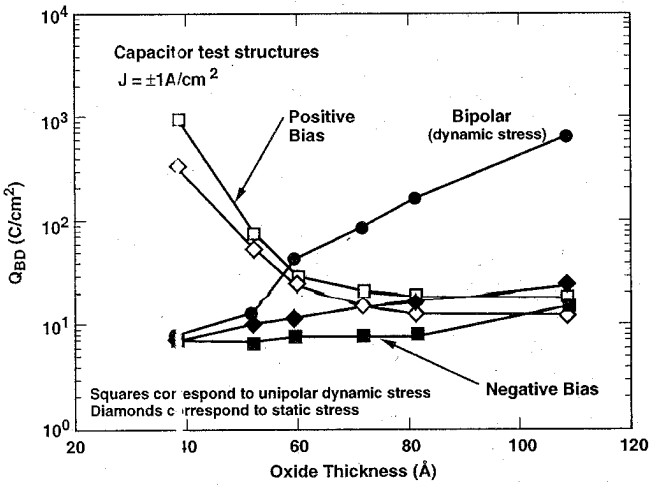

Figure 19. Effect of Stress Polarity on Charge to Breakdown for Various Oxide Thicknesses [59]

negative bias produced similar results. However, for thin. oxides there was a pronounced difference in Q_{BD} for positive and negative bias. They attributed this to differences in the surface roughness of the silicon and polysilicon regions that form the top and bottom of the capacitor.

Oxide breakdown is a complex topic. It is likely that impurities and defects play a role in gate rupture from heavy ions, but there are still uncertainties in the mechanism for breakdown and how it relates to conventional reliability considerations. Soft breakdown characteristics in thin oxides further complicate this problem.

D. Unresolved Issues and Future Work

Capacitors are useful vehicles to study breakdown. However, it is not at all obvious how one translates experimental work on large-area capacitors, which have simple, vertical structures, to small-area lateral transistor structures that have a very high transverse electric field, with non-planar construction. The net effect of the small currents produced by heavy ions may be different for small-area gates of MOS devices because of the strong lateral field. This may be one reason that the critical field of circuits is lower than that of capacitors.

The detailed mechanisms for gate rupture are also unresolved. Several ion strikes appear to be required to cause breakdown, both in capacitors and circuits. This may imply that the total injected charge is important, just as for reliability studies. On the other hand, it can also be explained if breakdown only occurs for ion strikes in close proximity to a defect, or to a localized region in a device structure with higher electric field.

Gate rupture is a fascinating topic for hardened technologies as well as commercial technologies. It is clearly an issue for devices with gate oxide thicknesses between 120 and 200 Å, where it occurs under normal bias conditions with field strengths far below the intrinsic breakdown limit or the reduced field strengths that are imposed by oxide reliability constraints.

More work needs to be done in order to determine how scaling affects this phenomenon. It may only be important for an intermediate range of scaled devices, just as for the microdose problem. However, gate rupture is a more severe issue because it can occur in random logic, and does not recover (anneal). The increasing number of transistors on individual circuits will also affect its importance in the future, particularly for circuit functions that are not amenable to error-correction-and-detection.

VIII. Device Architecture

We are used to thinking about semiconductor devices in rather simple terms. For example, semiconductor memories are generally considered to be a basic array of storage cells with relatively straightforward interface and control circuitry. This in turn leads to the concept of a threshold LET for cell upset, which gradually increases to a saturated value as the LET increases. The upset cross section of the complete circuit is expected to be a superposition of the upset cross section of individual cells.

As devices are scaled further, this concept will no longer be applicable because of new circuit design architectures that are required to cope with the limitations of leakage current, power dissipation, and speed that are major impediments to scaled devices. For example, to reduce power drain, future DRAMs have been proposed that subdivide the memory array into blocks [60,61]. Figure 20 shows an example. Only the block that is currently active is powered; the remaining blocks are turned off. Far more complex circuit architecture is required for such circuits, using internal state machines to control access to blocks, temporary registers to queue data and operational instructions, and methods to identify defective regions of the memory. The result is that the memory begins to look more like a microprocessor than a basic memory; the net effect is likely to make it extremely difficult to characterize the response of such devices and to deal with it in system applications. Similar effects have been seen in flash memories, which have adopted complex block-control and state-machine architectures.

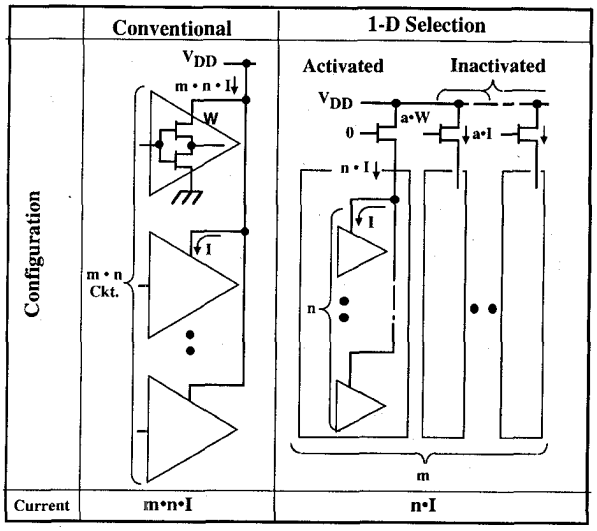

Figure 20. Block Architecture Proposed for 64-Mb DRAMs [59].

Another approach to increase storage density is that of storing more than one bit within each cell. An architecture with four different logic levels has been demonstrated for a 4-Gb DRAM [62]. Such designs require sense amplifiers that are capable of detecting different levels, essentially combining some aspects of analog design within the digital architecture. These examples suggest that dramatically different architectures are likely to be used in future memory technologies that may respond quite differently to ionizing radiation and single-event upset compared to traditional memory designs.

IX. Conclusions

Device scaling is a complicated issue that is progressing at a rapid pace. Four fundamental scaling issues – subthreshold slope, statistical variations in threshold voltage, substrate technology, and oxide field strength -- are likely to have major effects on the radiation response of scaled devices.

From the standpoint of gate threshold shifts, total dose performance is markedly improved by scaling even though the circuit tolerance for threshold variations is reduced for the lower logic levels in devices with lower power supply voltage. Field oxides appear to be the dominant issue for total dose hardness. More compact field isolation structures are required for scaled devices, which are likely to be more sensitive to leakage current and inversion than conventional LOCOS isolation. Charge pump circuits are another important issue for some circuit designs.

The SEU sensitivity of many commercial technologies appear to be close to the limit imposed by alpha particles. Although that results in a very low threshold LET, it is unlikely to get any worse as devices are scaled further. Many commercial technologies can be used in space in spite of this extreme sensitivity, as long as their response is predictable and consistent with system solutions, such as redundant parallel architectures or error detection and correction.

SEU-hardened devices will be required for key functions, such as microprocessors. Work on hardened devices shows that charge collection processes are far more complex than that assumed by older modeling approaches. Three-dimensional modeling is generally required to develop SEU-hardened structures in small devices. Simulations show that the device response is anisotropic, which affects error rate calculations as well as device design.

Latchup is expected to continue to be an important limitation as device technology evolves. Although the latchup immunity of many current technology circuits has been markedly improved by the use of very thin epitaxial layers on heavily doped substrates, there are cases where scaled devices are extremely vulnerable to latchup in spite of epitaxial construction. General scaling predictions are not possible for latchup because so many factors influence latchup sensitivity.

Finally, scaled devices that are exposed to heavy ions can be affected by two types of hard errors. Microdose errors – due to localized hole traps from a single heavy particle – appear to be important only for certain types of designs that are sensitive to small current increases. Device scaling trends predict that microdose errors will no longer be a factor for devices with optimized power supply voltages below 2 V, although they may be quite important for voltages between 2 and 3.3 V.

Gate rupture errors are potentially more important because they can occur in random logic as well as in memory cells, as well as in hardened devices. Higher oxide fields are anticipated for scaled devices which may make the gate rupture problem far more significant in the future. It is also possible that improvements in oxide quality may reduce its importance for extremely thin oxides. More work needs to be done on this topic to improve our understanding of the mechanisms, and also to determine how conventional reliability studies relate to gate-rupture sensitivity.

Acknowledgment

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References

[1] R. H. Dennard, F. H. Gaensslen, H-N. Yu, V. L. Rideout, E. Bassous and A. R. LeBlanc, "Design of Ion-Implanted MOSFETs with Very Small Physical Dimension," IEEE J. Solid State Circuits, SC-9, 256 (1974).

[2] G. Baccarini, M. R. Wordeman and R. H. Dennard, "Generalized Scaling Theory and Its Application to a 1/4 Micrometer MOSFET Design," IEEE Trans. Elect.. Dev., ED-31, 452 (1984).

[3] B. Davari, W-H. Chang, K. E. Petrillo, C. Y. Wong, D. Moy. Y. Taur, M. R. Wordeman, J. Y-C. Sun, C. C-H. Hsu and M. R. Polcari, "A High-Performance 0.25-μm CMOS Technology: II -- Technology," IEEE Trans. Elect. Dev., ED-39, 967 (1992).

[4] M. Nagata, "Limitations, Innovations, and Challenges of Circuits and Devices into a Half Micrometer and Beyond," IEEE J. of Solid-State Circuits, 27, 465 (1992).

[5] B. Davari, R. H. Dennard and G. G. Shahadi, "CMOS Scaling for High Perfromance and Low Power -- The Next Ten Years," Proc. of the IEEE, 83, 595 (1995).

[6] C. Hu, "Future CMOS Scaling and Reliability," Proc. of the IEEE, 81, 682 (1993).

[7] S. Asai and Y. Wada, "Technology Challenges for Integration Near and Below 0.1 μm," Proc. of the IEEE, 85, 505 (1997).

[8] C. Fiegna, H. Iwai, T. Wada, M. Saito, E. Sangiorgi and B. Ricco, "Scaling the MOS Transistor Below 0.1 μm: Methodology, Device Structures amd Technology Requirements," IEEE Trans. Elect. Dev., ED-41, 941 (1994).

[9] P. K. Rey, R. H. Doklan, E. P. Martin, S. F. Shive and A. K. Sinha, "Synthesis and Characterization of High Quality Ultrathin Gate Oxides for VLSI/ULSI Circuits, 1988 IDEM Technical Digest, p. 714.

[10] X. Tang, V. K. De and J. D. Meindl, "Intrinsic MOSFET Parameter Fluctuations Due to Random Dopant Placement," IEEE Trans. on VLSI Systems, 4, 369 (1997).

[11] Y. Taur, Y.-J. Mi, D. J. Frank, H.-S. Wong, D. A. Buchanan, S. J. Wind, S. A. Rishton, G. A. Sai-Halasz, and E. J. Nowak, "CMOS Scaling into the 21st Century and Beyond," IBM J. Res. Develop., 39, 245 (1995).

[12] K. Itoh, K. Sasaki and Y. Nakagome, "Trends in Low-Power RAM Circuit Technologies," Proc. of the IEEE, 83, 524 (1995).

[13] T. Sakata, K. Itoh, M. Horiguchi and M. Aoki, "Subthreshold Current Reduction Circuits for Multi-Gigabit DRAMs," IEEE J. Solid-State Circuits, 29, 761 (1994).

[14] C. Lage, D. Burnett, T. McNelly, K. Baker, A. Borman, D. Dreier and V. Soorholtz, "Soft Error Rate and Stored Charge Requirements in Advanced High-Density SRAMs," 1993 IEDM Technical Digest, p. 821.

[15] L. Lantz, III, "Soft Errors Induced by Alpha Particles," IEEE Trans. Reliability, 45, 174 (1996).

[16] T. P. Ma and P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*, Wiley Interscience, New York, 1989.

[17] N. S. Saks, M. G. Ancona and J. A. Modola, "Radiation Effects in MOS Capacitors with Very Thin Oxides at 80 K," IEEE Trans. Nucl. Sci., NS-31, 1249 (1984).

[18] A. Scarpa, R. Paccagnella, F. Montera, G. Ghibaudo, G. Pananakakis, G. Ghidini and P. G. Fuochi, "Ionizing Radidation Induced Leakage Current on Ultra-Thin Gate Oxides," IEEE Trans. Nucl. Sei., NS-44, 1818, 1997.

[19] R. Katz, G. Swift and D. Shaw, "Total Dose Responses of ACTEL 1020B and 1280A Field Programmable Gate Arrays," RADECS95 Proceedings, 412, IEEE Doc. 95TH8147.

[20] R. Escoffier, A. Michez, C. Cirba, G. Bordure, V. Ferlet-Cavrois, P. Paillet and J. L. Leray, "Radiation Induced Shift Study in Parametric MOS Structures by 2D Numerical Simulation," RADECS95 Proceedings, 45, IEEE Doc. 95TH8147.

[21] C. Brisset, V. Ferlet-Cavrois, O. Flament, O. Musseau, J. L. Leray, J. L. Pelloie, R. Escoffier, A. Michez, C. Cirba and G. Bordure, "Two-Dimensional Simulation of Total Dose Effects on NMOSFET with Lateral Parasitic Transistor," IEEE Trans. Nucl. Sci., NS-43, 2651 (1996).

[22] O. Flament, J. L. Autran, P. Paillet, P. Roche, O. Faynot and R. Truche, "Charge Pumping Analysis of Radiation Effects in LOCOS Parasitic Transistors," IEEE Trans. Nucl. Sei., NS-44, 1930 (1997).

[23] N. Shizumi, Y. Naito, Y. Itoh, Y. Shibata, K. Hashimoto, M. Nishio, A. Asai, K. Ohe, H. Umimoto and Y. Hirofuji, "A Poly-buffer Recessed LOCOS Process for 256 Mbit DRAM Cells," 1992 IEDM Technical Digest, p. 279

[24] S. S. Roth, W. J. Ray, C. Mazure, K. Cooper, H. Kirsch, C. D. Gunderson and J. Ko, "Characterization of Polysilicon-Encapsulated Local Oxidation," IEEE Trans. Elect. Dev., ED-39, 1085 (1992).

[25] A. Bryant, W. Hänsch and T. Mii, "Characteristics of CMOS Device Isolation for the ULSI Age," 1994 IEDM Technical Digest, p. 671.

[26] J. C. Pickel, "Single-Event Rate Calculations," IEEE Trans. Nucl. Sci., NS-43, 483 (1996).

[27] E. L. Petersen, "Approaches to Proton Single-Event Rate Calculations," IEEE Trans. Nucl. Sci., NS-43, 496 (1996).

[28] E. L. Petersen, P. Shapiro, J. H. Adams, Jr., and E. A. Burke, "Calculation of Cosmic-Ray Induced Soft Upset and Scaling in VLSI Devices," IEEE Trans. Nucl. Sci. NS-29, 2055 (1982).

[29] R. Velazco, S. Karoui and T. Chapuis, "SEU Testing of 32-bit Microprocessors," 1992 IEEE Radiation Effects Data Workshop, p. 16, IEEE Doc. 92TH0507-4.

[30] R. Harboe-Sorenson, L Adams, E. J. Day, C. Sanosoe, D. Mapper and T. K. Sanderson, ""The SEU Risk Assessment of Z80A, 8086 and 80C86 Microprocessors on a Low Altitude Polar Environment," IEEE Trans. Nucl. Sci., NS-33, 1626 (1986).

[31] C. K. Kouba, "Single Event Upset Characterizatics of the 486-DX4 Microprocessor," paper W-8, presented in the Data Workshop at the 1997 Nuclear and Space Radiation Effects Conference, Snowmass, Coloraodo, July 22-25, 1997.

[32] K. A. LaBel, A. K. Maron, D. K. Hawkins, A. B. Sanders, C. M. Siedleck, H. S. Kim, J. E. Forney, E. G. Stassinopoulos, P. Marshall, C. Dale and J. Kinnison, "Current Single Event Test Results for Candidate Spacecraft Electronics," 1996 IEEE Radiation Effects Data Workshop, p. 19, IEEE Doc. 96TH8199.

[33] F. Estreme, T. Chapuis, R. Velazco, S. Karoui, R. Trigauz, D. Benezech and L. H.. Rosier, "SEU and Latchup Results for SPARC Processors," 1993 IEEE Radiation Effects Data Workshop, p. 13, IEEE Doc. 93TH0657-7.

[34] F. Bezzera, S. Barde, R. Ecoffet, S. Fourtine, J. Barboule, M. Calvet, B. Gagnou, P. Leconte, P. Calvel and D. Hardy, "Radiation Tests of Commercial Microprocessors," paper W-9 of the Data Workshop at RADECS97, Cannes, France, September 17, 1997.

[35] O. Musseau, F. Gardic, P. Roche, T. Corbière, R. Reed, S. Buchner, P. McDonald, J. Melinger, L. Tran and A. Campbell, "Analysis of Multiple-Bit Upsets (MBU) in a CMOS RAM," IEEE Trans. Nucl. Sci., NS-43, 2879 (1996).

[36] L. W. Massengill, "Cosmic and Terrestrial Single-Event Radiation Effects in Dynamic Random Access Memories," IEEE Trans. Nucl. Sci., NS-43, 576 (1996).

[37] P. E. Dodd, Device Simulation of Charge Collection and Single Event Upset," IEEE Trans. Nucl. Sci., NS-43, 561 (1996).

[38] R. L. Woodruff and P. J. Rudeck, "Three-Dimensional Numerical Simulation of Single Event Upset of an SRAM Cell," IEEE Trans. Nucl. Sci., NS-40, 1795 (1993).

[39] S. Velacheri, L. W. Massengill and S. E. Kerns, "Single-Event Charge Collection and Direct Channel Conduction in Submicron Microcircuits," IEEE Trans. Nucl. Sci., NS-41, 2103 (1994).

[40] P. E. Dodd, F. W. Sexton, G. L. Hash, M. R. Shaneyfelt, B. L. Draper, A. J. Farino and R. S. Flores, "Impact of Technology Trends on SEU in CMOS SRAMs," IEEE Trans. Nucl. Sci., NS-43, 2797 (1996).

[41] Y. Moreau, S. Duzellier and J. Gasiot, "Evaluation of the Upset Risk in CMOS SRAM through Full Three Dimensional Simulation," IEEE Trans. Nucl. Sci., NS-42, 1789 (1995).

[42] D. Bessot and R. Velazco, "Design of SEU-Hardened CMOS Memory Cells: The Hit Cell," RADECS93 Proceedings, 563, IEEE Doc. 93TH0616-3.

[43] V. Lasserre, T. Corbière, B. Thomas and K. Rödde, "A Radiation Tolerant 0.6 μm Technology," RADECS95 Proceedings, 125, IEEE Doc. 95TH8147.

[44] O. Musseau, "Single-Event Effects in SOI Technologies and Devices," IEEE Trans. Nucl. Sci., NS-43, 603 (1996).

[45] T. Chapuis, H. Constans-Erems and L. Rosier, "Latchup on CMOS/EPI Devices," IEEE Trans. Nucl. Sci., NS-37, 839 (1990).

[46] A. H. Johnston, G. M. Swift, and L. D. Edmonds, "Latchup in Integrated Circuits from Energetic Protons," IEEE Trans. Nucl. Sei., NS-44, 2367, 1997.

[47] R. R. Troutman, *Latchup in CMOS Technology: The Problem and Its Cure*, Kluwer Academic Publishers, Norwalk, MA, 1986.

[48] G. Bruguier and J-M. Palau, "Single Particle-Induced Latchup," IEEE Trans. Nucl. Sci., NS-43, 522 (1996).

[49] A. H. Johnston, "The Influence of Technology Evolution on Radiation-Induced Latchup," IEEE Trans. Nucl. Sci., NS-43, 505 (1996).

[50] R. Koga, W. R. Crain, K. B. Crawford, D. D. Lau, S. D. Pinkerton, B. K. Yi and R. Chitty, "On the Suitability of Non-Hardened High Density SRAMs for Space Applications," IEEE Trans. Nucl. Sci., NS-38, 1507 (1991)

[51] C. Dufour, P. Garnier, T. Carrière, J. Beaucour, R. Ecoffet and M. Labrunèe, "Heavy-Ion Induced Single Hard Errors on Submicronic Memories," IEEE Trans. Nucl. Sci., NS-39, 1693 (1992).

[52] T. R. Oldham, K. W. Bennett, J. Beaucour, T. Carrière, C. Poivey and P. Garnier, "Total-Dose Failures in Advanced Electronics from Single Ions," IEEE Trans. Nucl. Sci., NS-40, 1820 (1993).

[53] G. M. Swift, D. J. Padgett and A. H. Johnston, "A New Class of Single Event Hard Errors," IEEE Trans. Nucl. Sci., NS-41, 2043 (1994).

[54] G. Swift and R. Katz, "An Experimental Survey of Heavy Ion Induced Gate Rupture in Actel Field Programmable Gate Arrays," RADECS95 Proceedings, 425, IEEE Doc. 95TH8147.

[55] A. H. Johnston, C. I. Lee, B. G. Rax and D. C. Shaw, "Using Commercial Technologies in Space," RADECS95 Proceedings, 175, IEEE Doc. 95TH8147.

[56] F. W. Sexton, D. M. Fleetwood, M. R. Shaneyfelt, P. E. Dodd, and G. L. Hash, "Single Event Gate Rupture in Thin Gate Oxides," IEEE Trans. Nucl. Sei., NS-44, 2345, 1997.

[57] M. Depas, T. Nigam and M. M. Heyns, "Soft Breakdown of Ultra-Thin Oxide Layers,," IEEE Trans. Elect. Dev., ED-43, 1419 (1996).

[58] C. Hu, "Gate Oxide Scaling Limits and Projections,"1996 IEDM Technical Digest, 319.

[59] H. Hwang and J. Lee, "Anomalous Breakdown Behavior in Ultrathin Oxides and Oxynitrides Under Dynamic Electrical Stress," IEEE Elect. Dev. Lett., EDL-13, 485 (1992).

[60] K. Itoh, K. Sasaki and Y. Nakagome, "Trends in Low-Power RAM Circuit Technologies," Proc. of the IEEE, 83, 524 (1995).

[61] J-H. Yoo, C-H. Kim, K-C. Lee, k-H. Kyung, S-M. Yoo, J-H. Lee, M-H. Son, J-M. Han, B-M. Kang, E. Haq, S-B. Lee, J-H. Sim, J-H. Dim, B-S. Moon, K-Y. Kim, J-G. Park, K-P. Lee, K-Y. Lee, K-N. Kim, S-I. Cho, J-W. Park and H-Y. Lim, "A 32-Bank 1 Gb DRAM with 1 GB/s Bandwidth," 1996 ISSC Tech. Digest, p. 378.

[62] T. Murotoni, I. Naritake, T. Matano, T. Ohtsuki, N. Kasai, H. Koga, K. Koyama, K. Nakajima, H. Yamaguchi, H. Watanabe and T. Okuda, "A 4-Level Storage 4Gb DRAM," 1997 ISSC Tech. Digest, p. 74.